UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/161,699	09/29/98	KIMURA K	Q49742

WM02/0405
SUGHRUE MION ZINN MACPEAK AND SEAS
2100 PENNSYLVANIA AVENUE NW
WASHINGTON DC 20037-3202

EXAMINER	
FATAHI YAR,M	
ART UNIT	**PAPER NUMBER**
2674	9

DATE MAILED: 04/05/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/161,699	Applicant(s) Kimura
	Examiner M. Fatahiyar	Group Art Unit 2674

☑ Responsive to communication(s) filed on Jan/3/01.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire three month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☑ Claim(s) 2-6 and 8-27 is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☑ Claim(s) 2-6 and 8-27 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☐ Notice of References Cited, PTO-892

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

— SEE OFFICE ACTION ON THE FOLLOWING PAGES —

1. Claims 17-26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In the claims 17-26, there is no antecedent basis for "the ferromagnetic FET". Correction and/or clarification is required.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

3. Claims 2-4, 8-10, 12 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Nakai et al. (6,072,454).

Nakai et al disclose a two-dimensional active-matrix type light modulation device comprising a plurality of pixel electrode arranged in the form of a two-dimensional matrix (106); a plurality of counter electrodes (106); a plurality of light modulating layers (106) interposed between the pixel electrodes and the counter electrodes and a drive circuit (101, 104, 105) constituted by ferroelectric gate field-effect transistors (104 and 105) connected to pixel electrodes wherein the drive circuit

writes data to the ferroelectric gate field-effect transistors in order of a row (102; column 14, lines 29-38).

In claims 2, 4, 10 and 12, as to the limitation "first and second polarization state", Nakai et al also teaches that the switching of the ferroelectric gate field-effect transistors for writing data in accordance with the input data is changed with the polarization state of the ferroelectric gate FET (see column 4, lines 56-60; column 5, lines 28-34; column 10, lines 59-62; column 12, lines 63-67).

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 5-6, 11, 13-14 and 16-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakai et al in view of Okumura et al. (6,115,018).

Nakai et al is discussed above. Okumura et al is cited to show that the concept of broadly utilizing a drive circuit consisting of a <u>single</u> TFT transistor (14) connected to a pixel electrode wherein the drive circuit performs row selection with a

gate electrode of the transistor and writes data with a source electrode and drain electrode of the transistor is old (see figure 1). Thus, it would have been obvious to one of ordinary skill in the art to modify the system of Nakai et al such that to only utilize a single ferroelectric gate field-effect transistor (104 and 105) wherein the drive circuit performs row selection with a gate electrode and writes data with a source electrode and drain electrode of the transistor (104 or 105), as evidenced by Okumura et al, because both references are directed to two-dimensional active-matrix type light modulation device.

As to claims 6 and 14, relative to the limitation "modulation by binary static drive", while Nakai et al do not explicitly specify "modulation by binary static drive" in their disclosure, but it is noted that their system is capable of performing gradation or halftoning for providing a multi-gradation display (column 21, lines 28-30; column 23, lines 47-54). Therefore, it would have been obvious to one of ordinary skill in the art to modify the system of Nakai et al such that the drive circuit perform modulation by binary static drive because "binary static drive" is considered to be an alternative equivalent driving technique for providing a multi-gradation display device.

7. Applicant's arguments with respect to claims 2-6 and 8-27 have been considered but are moot in view of the new ground(s) of rejection.

8. Any inquiry concerning this communication should be directed to M. Fatahiyar at telephone number (703) 305-6911.

MF/ayc MF

March 28, 2001

RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600